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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,546	03/23/2004	Lee D. Whetsel	TI-31203.1	2496

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EXAMINER	
NGUYEN, JIMMY	
ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,546	WHETSEL, LEE D.	
	Examiner	Art Unit	
	Jimmy Nguyen	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 – 5, 7 – 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii et al (US 5,434,513).

As to claims 1, **4**, Fujii et al disclose (fig 1) a wafer test system comprising:

A wafer (W) having a plurality of die to be tested,

a tester (connected to cable 35, column 4 line 3) having stimulus and response outputs,

and a connection (by pogo pins and switching circuit 25) formed between said plurality of die and tester outputs.

As to claims 2, **5**, Fujii et al disclose (fig 1) a process of testing die on wafer, comprising the steps of:

contacting the die (on W) with a tester (connected to cable 35, column 4 line 3),

and inputting test stimulus and response data from the tester (connected to cable 35, column 4 line 3).

As to claim 3, Fujii et al disclose (fig 1) a process of testing die on wafer, comprising the steps of:

probing the wafer (W) using only the number of probe 22) contacts required for testing a single die,

and testing a plurality of die (on W) simultaneously using only said number of probe contacts (22).

As to claims 7, 9, Fujii et al disclose (fig 1) a process of testing an integrated circuit comprising the steps of:

inputting test stimulus and response data (from the tester, (connected to cable 35, column 4 line 3), to said integrated circuit (on W),

and reading pass/fail (from the tester, connected to cable 35, column 4 line 3),information from the integrated circuit.

As to claim 8, Fujii et al disclose (fig 1) an integrated circuit tester comprising:

outputs (from the tester) for inputting stimulus data (providing input) to an integrated circuit (on W),

and outputs for inputting response data to an integrated circuit (on W).

As to claims 10, 11, Fujii et al disclose (fig 1) a semiconductor wafer comprising:

a plurality of identical die formed on the wafer (W), each die having a common set of input and output pads (13),

and a plurality of connections formed on the wafer (W), ones of said plurality of connections forming unique electrical connections between said common die input pads (13) and unique electrical connections between said common die output pads (13).

3. Claim 6 is rejected under 35 U.S.C. 102(b) as being anticipated by Garnett (US 5,912,563).

As to claim 6, Garnett discloses (fig 1) an integrated circuit comprising at least one test circuit, said test circuit comprising:

a trinary gate (Vh, Vl, mid) ,

a compare circuit (16, 18),

and a fail flag memory (24).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy Nguyen whose telephone number is 571-272-1965. The examiner can normally be reached on M-F from 9 to 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ramtez Nestor, can be reached on 571 –272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jimmy Nguyen

9/16/05

VINH NGUYEN
PRIMARY EXAMINER
A.U. 2829
09/17/05